Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **V IN (2 bond pads)**
2. **V OUT (2 bond pads)**
3. **V OUT SENSE**
4. **ADJUST**

**.086”**

**.093”**

**DIE ID**

**1**

**1**

**7**

**C**

**1**

**2**

**2**

**1**

**3**

**4**

**Notes:**

**For operation to specification, chip back should be connected to V OUT**

**For 3 pin applications, connect V OUT SENSE to V OUT**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004” min**

**Backside Potential: Vout**

**Mask Ref: 117C**

**APPROVED BY: DK DIE SIZE .086” X .093” DATE: 8/30/21**

**MFG: NATIONAL SEMI THICKNESS .011” P/N: LM117K**

**DG 10.1.2**

#### Rev B, 7/19/02